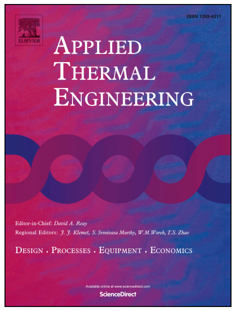


Impact of the Substrate on the Efficiency of Thin Film Thermoelectric Technology


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PII: S1359-4311(15)00286-0

DOI: 10.1016/j.applthermaleng.2015.03.062

Reference: ATE 6497

To appear in: *Applied Thermal Engineering*

Received Date: 12 February 2015

Accepted Date: 26 March 2015

# Impact of the Substrate on the Efficiency of Thin Film Thermoelectric Technology

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**Abstract**

Thermoelectricity is one of the simplest technologies for thermal energy conversion. Moreover, because of their relatively low efficiency, bulk thermoelectric materials are generally used in environments where their solid state nature outweighs their poor efficiency. Nevertheless, low dimensional thermoelectric materials shed a light in order to achieve higher thermoelectric performance than their bulk counterparts via quantum and spatial confinement of energy carriers. The Thermoelectric figure of merit *ZT* is the basic criterion for estimating the performance of thermoelectric materials. In this work, by way of an extension of the Harman method to thin films onto substrate to evaluate *ZT* it is shown that the solely presence of a substrate affects significantly the intrinsic value of the *ZT* independently of the electrical and thermal nature of the substrate. Furthermore, the model unveils that as the thickness ratio between substrate and thin film increases, the parameter *ZT* sharply tends to zero; this effect opens a serious problem to overcome by the thin film thermoelectric technology, especially at nanoscale. In this sense, challenges in order to engineering planar thermoelectric devices at micro/nanoscale are properly identified.

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## I. Introduction

Thermoelectric materials can generate electrical power from heat, and use electricity to work as heat pumps providing active cooling or heating. The low efficiency of devices based on common bulk thermoelectric materials confine their applications to niches in which their advantages in compactness, environmentally friendly and free maintenance outweigh its poor efficiency. Although in the past the applications of thermoelectric systems were limited to niche applications, now the motivation is different and with significant improvements in thermoelectric technology, interest in hot spot computer processors thermoelectric cooling and waste heat vehicle recovery systems is more widespread [1, 2 and references therein].

Recent developments in nanotechnologies have led significant *ZT* enhancement in two-dimensional (thin films) and one-dimensional (nanowires) thermoelectric materials [3-8].

Low-dimensional thermoelectric materials accomplish higher thermoelectric properties than their bulk counterparts via two mechanisms: quantum confinement and spatial confinement of the energy carriers. In the first approach an increase of the thermopower can be obtained by enhancing the density of states near Fermi level via quantum confinement; in the second approach, phonons over a large mean free path range can be effectively confined inside of the thin film because thickness of the thin film becomes smaller than phonon mean free path as well as due to an increase of phonon scattering at boundaries of material, hence resulting in the decrease of the lattice thermal conductivity [9-11]. In any case, is clear that the fundamental challenge involved in using thermoelectric devices is highly related with the improvement of the thermoelectric figure of merit of the material *ZT*.

Recently, planar thermoelectric microcoolers and microgenerators on flexible substrates are being developed in order to be integrated in wearable systems as well as to power up autonomous microsystems; in such systems the effect of the substrate nature on the thermoelectric figure of merit *ZT* is not taken in to consideration in the design of the thermoelectric device [12-15]. Instead, intrinsic values of *ZT* are reported for those thermoelectric thin films and devices; however, it is clear that in such systems the substrate represent a problem because it is impossible to deposit a thin film without substrate and generally this substrate is hundreds of times thicker than the thermoelectric film. Moreover, depending on the electrical and thermal nature of the substrate it might represent a thermal and/or electrical shunt for the thermoelectric thin film; as a consequence, an effective thermoelectric figure of merit lower than the intrinsic one is presented in the system, this effect opens a serious problem to overcome by the thin film thermoelectric technology, especially at nanoscale.

To measure the thermoelectric figure of merit $ZT = S^2\sigma T/k$ of a thermoelectric material a method originally proposed by Harman is commonly used [16]. In the method, the specimen under test must be a bulk thermoelectric material. A direct current $I$ is then passed through it by way of metal leads; as a result, a temperature difference is induced between the ends of the sample due to the Peltier effect. In this technique the Joule heating generated on the sample is considered to be equally distributed along the sample, thus this effect does not affect the Peltier temperature gradient, therefore the rate of heat current due to Peltier effect is given by $\dot{Q}_\Pi = \Pi I$ , where $\Pi$ is the Peltier coefficient. In addition to the Peltier effect, a thermoelectric voltage $V_{th}$ is generated on the ends of the sample due to Seebeck effect as shown in figure 1, this Seebeck coefficient is given by $S = \frac{\delta V_{Th}}{\delta T}$ .

The Peltier coefficient $\Pi$ and Seebeck coefficient $S$ are related by the Thomson relation $\Pi = ST$ , here $T$ is the absolute temperature. By combining the rate of heat current due to Peltier effect and the Thomson relation, we get

$$\dot{Q}_\Pi = STI \tag{1}$$

In order to maintain the thermal equilibrium it is necessary that the rate of heat flow arising from Peltier effect $\dot{Q}_\Pi$ must be balanced by an equal and opposite rate of heat flow due to sample thermal conduction $\dot{Q}_k$, then the rate of conduction heat current can be expressed from the Fourier law as

$$\dot{Q}_k = \frac{kA\delta T}{\delta x} \tag{2}$$

Equating equation (1) and equation (2), the steady state temperature gradient along the specimen is

$$\delta T = \frac{STI\delta x}{kA} \tag{3}$$

By combining equation (3) and the Seebeck coefficient, the thermoelectric voltage $V_{th}$ under adiabatic conditions across the sample is defined by

$$V_{Th} = \frac{S^2 TI\delta x}{kA} \tag{4}$$

Besides, the isothermal voltage is given by

$$V_{ISO} = IR \tag{5}$$

Therefore the total adiabatic voltage on the material is given by:

$$V_{AD} = V_{ISO} + V_{Th} = IR + \frac{S^2 TI\delta x}{kA} \tag{6}$$

By applying some algebra and rearranging terms

$$\frac{V_{AD}}{V_{ISO}} - 1 = ZT = \frac{S^2 \sigma T}{k} \tag{7}$$

Finally, from equation (7) the experimental figure of merit *ZT* of bulk materials by the Harman method can be determined by simply measuring the adiabatic and isothermal voltages.

## II. Extended Harman method to thin films onto substrate

*Case-1: In-plane ZT for thin film onto substrate*

If the thermoelectric thin film be deposited on the substrate, it is clear that the heat flow can flow in the plane through two different parallel paths; along the substrate and along the thin film, as you can see in figure 2a and 2b. It means that the portion of heat current in each material will depend on their thermal conductivities, thus some part of the heat current will leak to the substrate and therefore equation (7) is no longer valid to evaluate *ZT*.

In this situation, the rate of heat flux by conduction is given by

$$\dot{Q}_k = -\left[\frac{k_f A_f \delta T}{\delta x} + \frac{k_s A_s \delta T}{\delta x}\right] \tag{8}$$

Where $k_f$, $A_f$ and $k_s$, $A_s$ are the thermal conductivities and cross sections for the thin film and substrate respectively. Under steady state equilibrium condition $\dot{Q}_\Pi = \dot{Q}_k$ the in-plane temperature difference along the specimen is given by

$$\delta T = \frac{STI\delta x}{k_f at_f + k_s at_s} \tag{9}$$

Therefore, the thermoelectric adiabatic voltage is given by

$$\delta V_{Th} = \frac{S^2 TI\delta x}{k_f at_f + k_s at_s} \tag{10}$$

Taking into account an electrical current flowing through a parallel electrical path, the isothermal voltage is given by

$$\delta V_{ISO} = \frac{I\delta x}{\sigma_f at_f + \sigma_s at_s} \tag{11}$$

Where $\sigma_f$, $t_f$ and $\sigma_s$, $t_s$ are the electrical conductivities and thicknesses for the thin film and substrate respectively, *a* is the side of the sample.

Knowing that $V_{AD} = V_{ISO} + V_{Th}$ and combining equations (10) and (11) as well as applying some algebra then

$$\left[\frac{V_{AD}}{V_{ISO}} - 1\right] = ZT = \frac{S^2 T\sigma_f}{k_f + k_s \frac{t_s}{t_f}} + \frac{S^2 T\sigma_s \frac{t_s}{t_f}}{k_f + k_s \frac{t_s}{t_f}} \tag{12}$$

Where from analysis circuit theory

$$S = S_f + \frac{\sigma_s}{\sigma_s + \sigma_f}\left(S_s - S_f\right)$$

Using equation (12) it can be obtained the effective *ZT* from the experimental adiabatic and isothermal voltages for a thermoelectric thin film deposited onto substrate. It is clear that the thermal and electrical conductivity as well as the thickness of the substrate affects the *ZT* value of the single thin film.

In the event that the substrate is a dielectric material, then in the limit when $\sigma_s \rightarrow 0$ equation (12) reduces to

$$\left[\frac{V_{AD}}{V_{ISO}} - 1\right] = ZT = \frac{S^2 T\sigma_f}{k_f + k_s \frac{t_s}{t_f}} \tag{13}$$

Equation (13) gives the *ZT* for a thermoelectric thin film onto dielectric substrate; it can be observed that corrections can be done if the thermal conductivity and thickness of the substrate are known.

*Case-2: Cross-plane ZT for thin film onto substrate*

On the other hand, if the thermoelectric thin film be deposited on the substrate, it is clear that the cross-plane heat flow can flow through only one path; along the substrate-thin film system, as you can see in figure 3a and 3b. It means that the portion of heat current in each material is exactly the same and it will not depend on their thermal conductivities. Nevertheless, the temperature rise generated on the substrate will decreased the total temperature rise generated on the thin film; as a consequence equation (7) is no longer valid to evaluate *ZT* in such system.

Similarly, by simple energy balance as shown previously it can be demonstrated that the effective thermoelectric figure of merit *ZT* for cross plane configuration system is given by

$$\left[\frac{V_{AD}}{V_{ISO}} - 1\right] = ZT = \frac{S^2 T\sigma_f}{k_f + k_f \dfrac{\sigma_f}{\sigma_s}\dfrac{t_s}{t_f}} + \frac{S^2 T\sigma_f \dfrac{t_s}{t_f}}{k_s + k_s \dfrac{\sigma_f}{\sigma_s}\dfrac{t_s}{t_f}} \tag{14}$$

where from analysis circuit theory, $S = S_f + S_s$.

It is clear from figure 3 that in this configuration it is necessary a conducting substrate in order to measure the adiabatic and isothermal voltages in order to obtain the *ZT* by Harman method. In this case as expected, the thermal conductivity and thickness of the substrate influence the value of ZT.

## III. Modeling and Experimental Results

Figure 4 shows by way of modeling of equation (12) the effect of the thermal conductivity of the substrate on the figure of merit *ZT* of the Bi thin film when an in-plane heat flow is applied to such system. From calculations, evidently the figure of merit for a Bi thin film with not substrate is always constant, however if the same film is deposited onto substrate it is clear from the figure 4 that the thermal conductivity of the substrate affects the value *ZT*, for high thermal conductivity substrates this *ZT* value is highly decreased (i.e. intrinsic silicon substrates). Conversely, when the thermal conductivity of the substrate tends to decrease, the effective *ZT* of the system goes to high values; therefore low thermal conductivities substrates benefit the effective *ZT* of the system.

In addition, from the same figure 4, we can see that the thickness ratio between substrate and film ($X= t_s/t_f$) plays an important role on the effective value of *ZT*, for example if we deposit a 100nm Bi thin film onto 500μm Si wafer the thickness ratio X will be 5000, thus it can be seen in the figure that the effective value of *ZT* is highly effected and the system behaves like a non-thermoelectric system and it seems to be almost independent of the thermal conductivity of the substrate. On the contrary, if we decreased the thickness ratio to 50, the silicon substrate system does not experience significant changes; however low thermal conductivity substrates such as $SiO_2$ or Kapton benefits highly the effective *ZT* of the system for the same thickness ratio.

Figure 5 shows the effect of the electrical conductivity of the substrate. As example we model equation (12) for three different level of doping of Si substrates. It is clear from figure 5 that highly doped substrates tend to slightly increase the *ZT* of the system, this improvement of the *ZT* is mainly due to the reduction of the thermal conductivity of the substrate because the doping rather than the electrical conductivity. It is widely known that doping of semiconductors increase their electrical conductivity but decrease their thermal conductivity because phonons are highly scattered due to dopant atoms [17].

In order to prove the corrections suggested by equation (12) to the Harman method we have measured the *ZT* values for a 500nm Bi thin film deposited onto commercially available 25μm, 50μm, 75μm and 125μm Kapton sheets, with these values with get a 50, 100, 150 and 250 thickness ratios respectively. Bi thin films were deposited by e-beam evaporation from Bi pellets onto commercially available four different thickness Kapton sheets. The adiabatic voltage was measured with the Keithley 8221 Nanovoltmeter by applying a 10mA dc current by using the Keithley 6221 AC/DC current source. Moreover, the isothermal voltage was measured with SR830 lock-in amplifier by applying 10mA and 10Hz square wave (AC) by using the Keithley 6221 AC/DC current source.

To avoid heat conduction losses, a low thermal conductivity wire was used for wiring the sample. Thus, four Manganin wires of 50μm of diameter and 10cm length were attached to the samples with silver paste in a four point configuration. Next an AC squared wave current is applied during about 30 seconds and the isothermal voltage is measured, then the AC current is suddenly switched to a DC current during 30 seconds and the adiabatic voltage is measured.

By using this data the experimental effective *ZT* is obtained. All measurements were carried out at room temperature range (300 K) in a vacuum chamber of $5X10^{-6}$ mbar to minimize convection heat losses.

Experimental *ZT* results are presented in figure 6 as red star symbols. Solid black line represents the modeling of equation (12) for dielectric substrates (i.e. $\sigma_s=0$), and the constant blue solid line represents the expected value for the film without substrate. Evidently, the thinnest substrate shows the best *ZT* value. In general, as the substrate thickness increases the *ZT* value decreases. This figure 6 clearly unveils the problematic that faces the thin film thermoelectric technology, especially at nanoscale. In low dimensional systems of the order of nanometers the thickness ratio could be very large; for instance, a thermoelectric thin film of ten nanometers deposited onto a standard 500µm Si substrate will have a thickness ratio of 50000, thus independently of the *ZT* value of the film surely its effective *ZT* value will be very close to zero.

Table 1 shows the experimental data for *ZT*. Also corrected data are shown according to the corresponding corrections suggested by equation (12). The average value of the four corrected measurement gives a *ZT*=0.137, which is close to the 0.152 predicted value for equation (13) for a Bi thin film without substrate.

Moreover, if the heat flows through system in the cross-plane direction; according to equation (14) the use of conducting substrate is absolutely necessary $\sigma_s \neq 0$, and therefore dielectric substrates with low thermal conductivity do not benefit the *ZT* value as shown previously in the case of the in-plane heat flow system.

Nevertheless, electrical conductivity of the substrate in such systems plays an important role; for instance, in pure metals the condition $\sigma_s \rightarrow \infty$ does not exist rather they obey the Wiedemann-Franz law defined as $\sigma/k=LT$ where $L=2.45\text{x}10^{-8}$ $W\Omega/K^2$ is the Lorentz number. Therefore, the second term in equation (14) does not tend to zero and it can contribute or not to increase the *ZT* in such systems, mainly depending on the sign of the Seebeck voltage. Bi presents a N-type Seebeck coefficient, in this case a P-type substrate will reduce the effective *ZT*, however a N-type Seebeck coefficient substrate will increase the effective *ZT* of the system. In figure 7 it is shown the modeling of a Bi thin film deposited onto a P-type metallic substrate as well as a N-type highly doped Si substrate. It is clear from figure 7 that a highly doped Si substrate benefits to the effective *ZT* value because Seebeck voltage of doped Si is bigger than any metallic substrate (i.e. Al or Cu), therefore this plays in favor of the effective *ZT* of the cross plane configuration. Moreover, in figure 7 also is observed that low thickness ratios (very low thickness of the semiconducting substrates) could improve and even overcome the maximum *ZT* value for the Bi thin film without substrate; this is due to significant Seebeck voltage present on the semiconductor help increase *ZT* as explained above.

## IV. Conclusions

We have demonstrated by way of a modified version of the Harman method the problems to overcome in order to keep unaffected the thermoelectric figure of merit of planar devices.

The model takes the effects of the thermal and electrical nature of the substrate into account, as well as its thickness. Experimental results are consistent with the modeling and they show that the solely presence of a substrate affects significantly the intrinsic value of the figure of merit of the film independently of the substrate nature. Nevertheless, conducting thick substrates decrease more significantly the *ZT* value than dielectric thin ones in the in-plane configuration but not in the cross-plane. Furthermore, the model unveils that as the thickness ratio between substrate and thin film increases, the parameter *ZT* sharply tends to zero; this effect opens a serious problem to overcome by the thin film thermoelectric technology, especially at nanoscale.

**Acknowledgments**

This work was supported by CONACYT, the Mexican Council for Science and Technology through Grant for fundamental research No. 241597.

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## Figure Captions

Figure 1. a) Thermoelectric and b) Thermal assumed models for the analysis of the Harman method of bulk materials.

Figure 2. a) Thermoelectric and b) Thermal assumed models for the in-plane analysis of the thermoelectric thin film deposited onto substrate.

Figure 3. a) Thermoelectric and b) Thermal assumed models for the cross-plane analysis of the thermoelectric thin film deposited onto substrate.

Figure 4. Modeling of equation (12) [ZT vs $t_s/t_f$] for a Bismuth thin film deposited onto different thermal conductivities substrates.

Figure 5. Modeling of equation (12) [ZT vs. $t_s/t_f$] for a Bismuth thin film deposited onto different electrical conductivities substrates.

Figure 6. Experimental results of ZT vs $t_s/t_f$ , for a Bismuth thin film deposited onto different thickness of Kapton sheet substrates.

Figure 7. Modeling of equation (14) [ZT vs $t_s/t_f$] for a Bismuth thin film deposited onto different electrical conductivities substrates as well as different type of Seebeck voltages.

## Table Captions

Table 1. Experimental and corrected *ZT* values for a Bi Thin film deposited on kapton foil.

**Table 1**

| **Thickness ratio ($t_s/t_f$)** | **Effective ZT (experimental data)** | **Corrected ZT** |
|---|---|---|
| 50 | 0.0844 | 0.161 |
| 100 | 0.0595 | 0.128 |
| 150 | 0.0532 | 0.135 |
| 250 | 0.0401 | 0.127 |

**Figure 1**

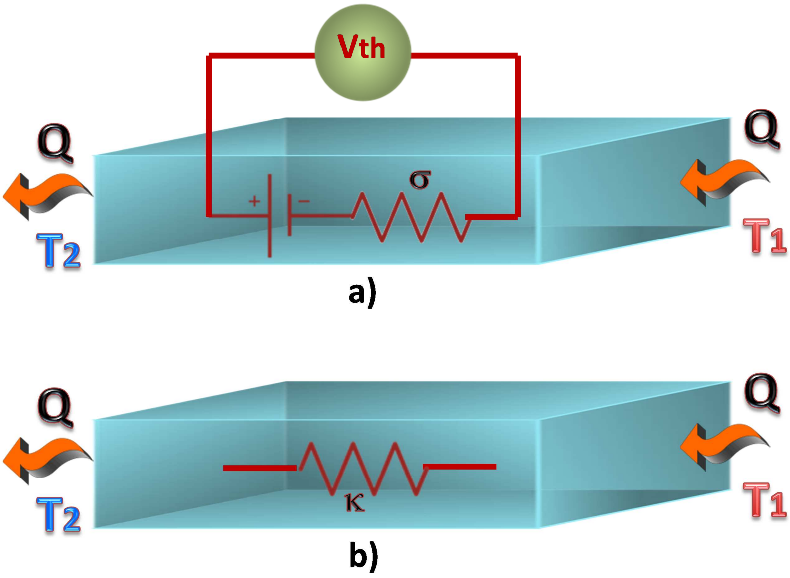


**Figure 2**

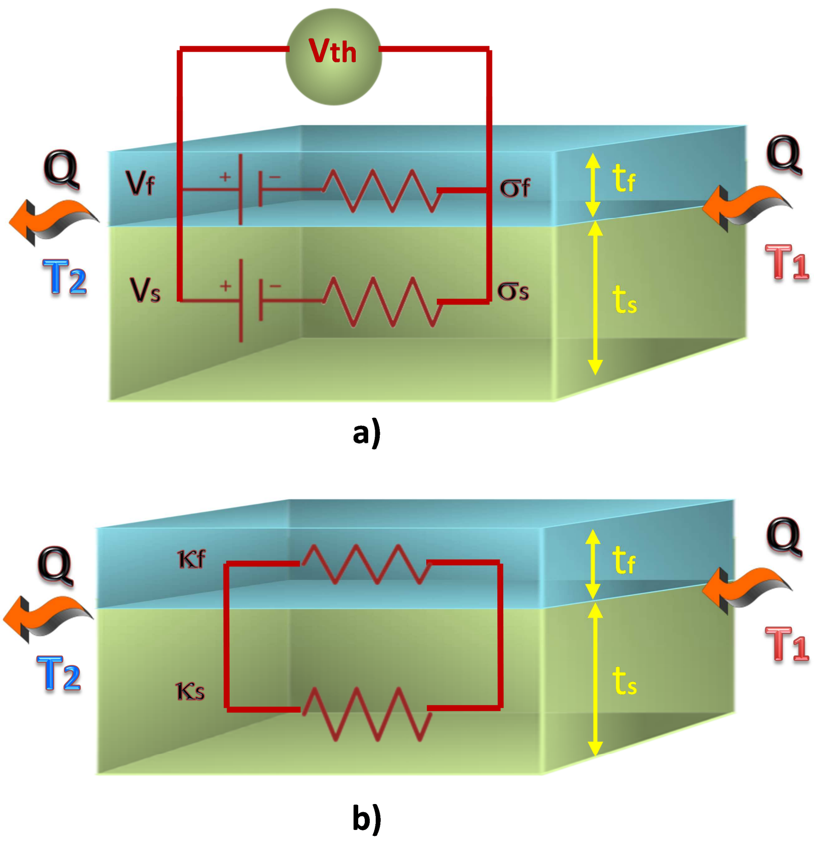


**Figure 3**

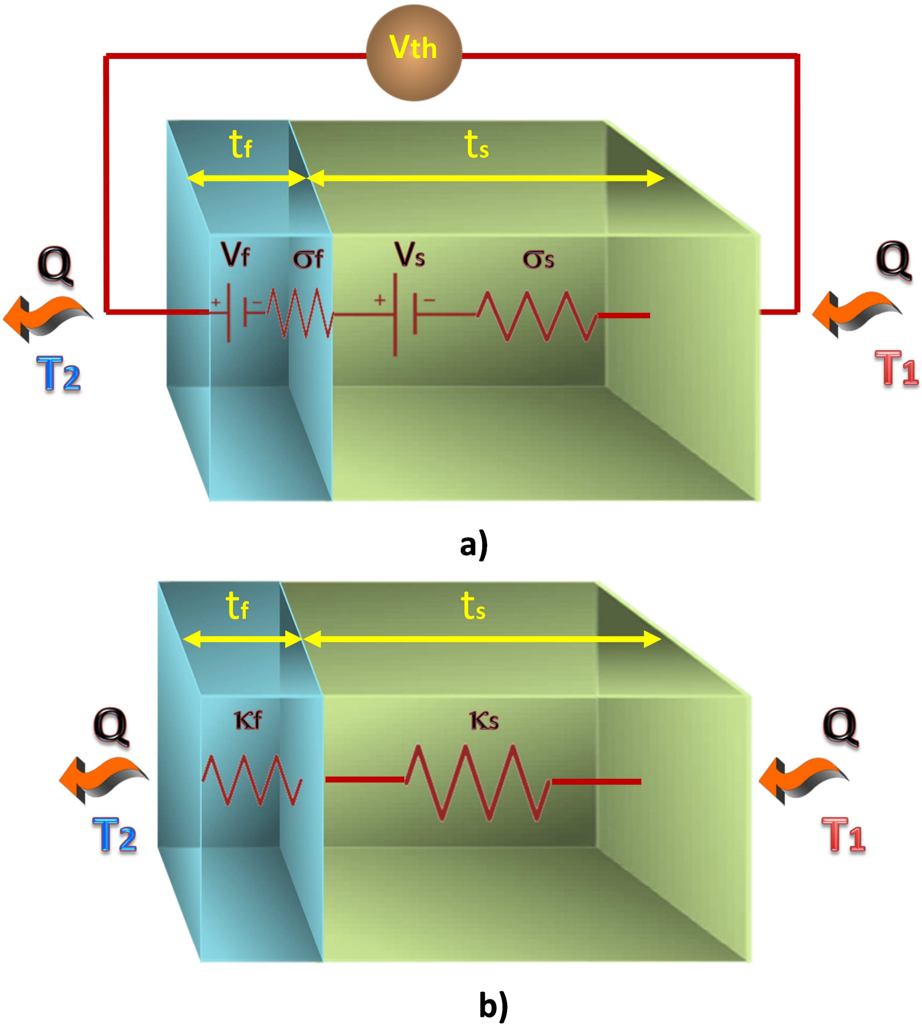
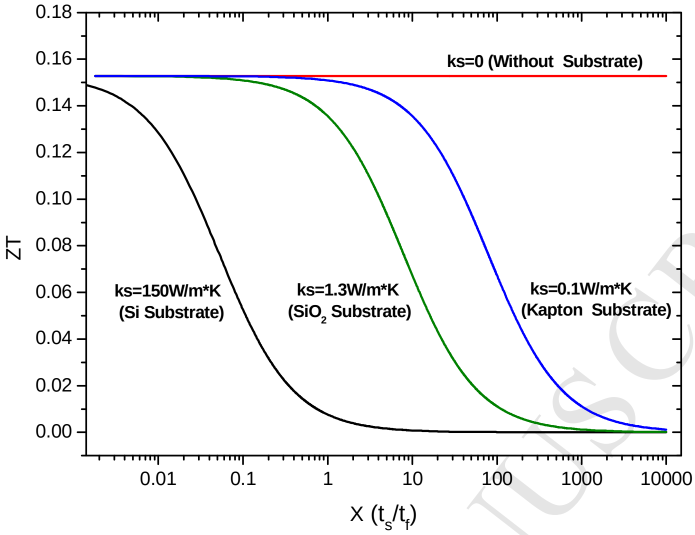


**Figure 4**


0.18
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0.10
0.08
0.06
0.04
0.02
0.00
ZT
ks=0 (Without Substrate)
ks=150W/m*K
(Si Substrate)
ks=1.3W/m*K
(SiO2 Substrate)
ks=0.1W/m*K
(Kapton Substrate)
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0.1
1
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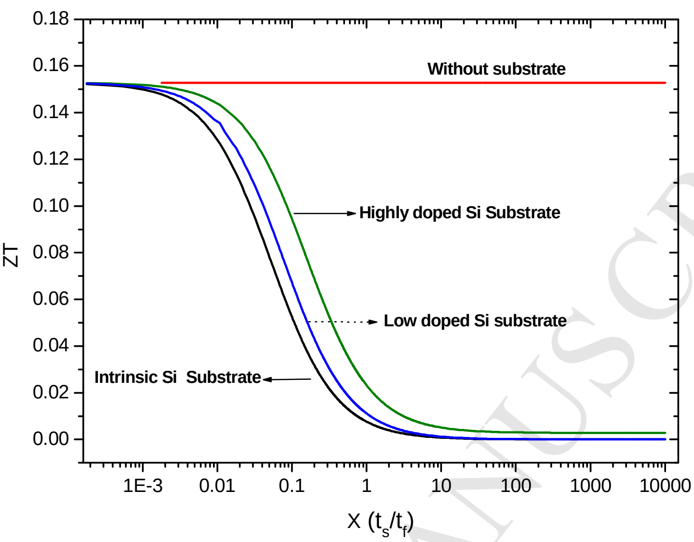
100
1000
10000
X (ts/tf)

**Figure 5**



ZT
0.18
0.16
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0.08
0.06
0.04
0.02
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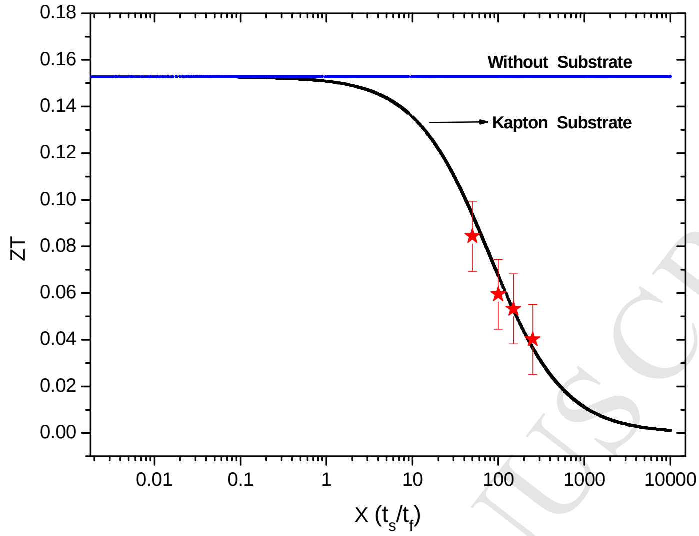
1E-3
0.01
0.1
1
10
100
1000
10000
X ($t_s/t_f$)
Without substrate
Highly doped Si Substrate
Low doped Si substrate
Intrinsic Si Substrate

**Figure 6**



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ZT
Without Substrate
Kapton Substrate
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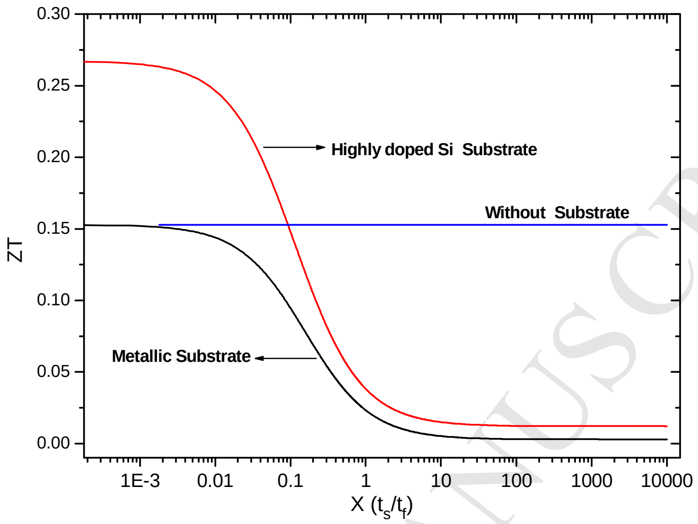
X ($t_s/t_f$)

**Figure 7**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ZT
Highly doped Si Substrate
Without Substrate
Metallic Substrate
1E-3
0.01
0.1
1
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100
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10000
X ($t_s/t_f$)

## Highlights

- Extended Harman method to evaluate ZT of thin films onto substrate is presented.
- ZT of thermoelectric thin films is strongly affected by substrate's nature.
- Thin dielectric substrates are desirable to hold ZT in in-plane configuration.
- Film/substrate thickness ratio play important role on the device performance.
- Challenges to engineering planar thermoelectric devices are properly identified.